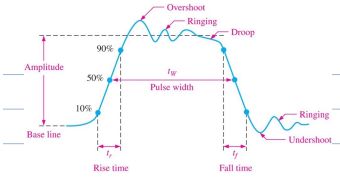
悬空为 1
active-LOW/HIGH



Rise time & Fall time 10% 90%

Pause width 50% 50%

Duty cycle $\frac{t_W}{T} \times 100\%$ Data transfer: { serial form / parallel form

Number system Dec. Bin. Oct. Hex. 1001 (MSB … LSB) Dec ⟶ Bin { Repeated Division-by-2 Method / Repeated Multiplication-by-2 Method

Complement of Binary Numbers

2's complement = 1's complement + 1

Sign-Magnitude form: The Sign Bit + The Magnitude Bits

1's Complement Form & 2's complement form: positive — same way

1's CF ⟶ Dec: − Sign bit × weight + Σ other bit × weight + 1 (when negative) → removed when 2's CF → Dec

e.g. $-5=(1111\,1010)_{2's} = -2^7+2^6+2^5+2^4+2^3+2^1+1$

Range -2^{n-1} to $2^{n-1}-1$ 8 bit ⟶ 1 byte

Arithmetic Operations with Signed Numbers

$[x+y]_{2c}=[x]_{2c}+[y]_{2c}$ discard any final bit; an overflow can occur when both + or −

subtraction: add the negative subtrahend (减数)

multiplication 1. Determine if the sign bits are same

2. change the form to the true form (for negative)

3. mult and add

4. add the sign bit and transform it to 2CF.

division: just using subtract

BCD (Binary-coded-decimal)

Always mean the 8421 code ⟶ 4-bit group

Addition: when it is invalid, just add 6: 0110

Excess three code

The Gray Code (a single bit change)

Bin-to-Gray e.g., 1 0 1 1 0 → 1 1 1 0 1 Gray-to-Bin e.g., 1 1 0 1 1 → 1 0 0 1 0

Even parity & odd parity: let the group always have even/odd 1s.

Boolean Algebra

Inverter — NOT; NAND Gate; NOR Gate

XOR (exclusive-OR) gate $X=\bar{A}B+A\bar{B}=A\oplus B$

XNOR (exclusive-NOR) gate $A\odot B$

complement, literal

product term, sum term

Commutative, Associative, Distributed, Identity, Weak, Idempotency, Involution, Adjacency, Absorption

$AA=A$, $A+A=A$; $\bar{\bar{A}}=A$; $A+\bar{A}B=A+B$, $A(\bar{A}+B)=AB$; $A+AB=A$, $A(A+B)=A$

Consensus $AB+\bar{A}C+BC=AB+\bar{A}C$

A standard POS — maxterm, SOP — minterm, Minimum SOP Expression

Negative-OR

The Universal of NAND & NOR — Negative-AND

Functions of Combinational Logic

Half Adder Full Adder C_n

Ripple carry adder & Carry Look-ahead { $C_n=G_{in}+P_nC_{n-1}$, $P_n=A_n\oplus B_n$, $G_n=AB$ / $\Sigma_n=P_n\oplus C_{n-1}$

Comparator 4-bit A>B A=B A<B

Decoder: The 4-Bit Decoder — 4-line-to-16-line

& Encoder

n input - 2^n output decoder & OR gate ⟶ implement n-variable logic function (minterm)

The BCD-to-Decimal Decoder

Multiplexer (MUX, Data Selectors) sometimes 4

8-input mux ⟶ implement specified 3-variable logic function

Demultiplexer (Demux), Parity Generators/Checkers

Latches

S-R Latch $\bar{S}$ $\bar{R}$ Q (active-LOW) Set & Reset $Q^{n+1}=\bar{S}+\bar{R}Q^n$

The gated { S-R / D (Data) } when EN is low, No change

Flip-Flops output changes state only at a specified point

The D Flip-Flop, Master-Slave Flip-Flop (CLK=1 期间主触发输出可能多次翻转), Edge-triggered operation

J-K Flip-Flop (J=Set, K=Reset, J=K=1 ⟶ Toggle) $Q^{n+1}=J\bar{Q}^n+\bar{K}Q^n$ Significant ☆

T Flip-Flop $Q^{n+1}=T\oplus Q^n$ (J=K=T), toggle when T=1 (also, $T=Q^{n+1}\oplus Q^n$)

Preset and Clear (PRE & CLR) asynchronous & synchronous ↘ instantly

Operating Characteristics:

Propagation Delay Times, Set-up Time, Hold Time

Application: Modulo 4 Counter, one-2^{nd} frequency;

Shift Registers — serial & parallel (不考)

Finite State Machine

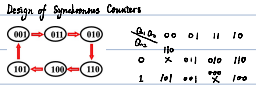
Counter:

Asynchronous 频率限制: $f_{max}=\frac{1}{N\tau_p}$ 前面输出作为后级的 CLK, 直接触发 Clear

Synchronous CLK-共 P T Q P=1时, Q反转 RCO输出为1时的条件: TC & ENP/ENT 会利用 Load

Up/down $J_i=(\ )\,UP+(\ )\,DOWN$

Design of Synchronous Counters 注2: just use Karnaugh map for each J_i, K_i, etc.



Q_1Q_0 / Q_2	00	01	11	10
0	110	X	011	010
1	101	001	000	X 100

(or using load. Hint: just change the difference.)

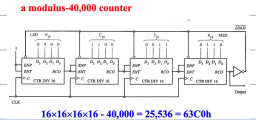
检验是否会自启动

$Q_2=\bar{Q}_0$, $Q_1=\bar{Q}_2$, $Q_0=Q_2\bar{Q}_1+Q_1Q_0=(Q_1+\bar{Q}_2)(Q_1+Q_0)Q_0+(Q_2+\bar{Q}_1)\bar{Q}_0$

One step: The logic diagram

(Hint: for UP/DOWN, add Y in Karnaugh map.)

a modulus-40,000 counter

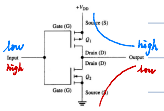


16×16×16×16 - 40,000 = 25,536 = 63C0h

using LOAD to implement a divide-by-40000 counter

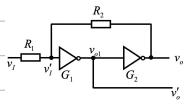
Glitch

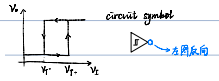
CMOS Inverter



Schmitt-Trigger

hysteresis





circuit symbol

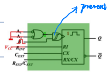
→ 左同反向

application :

pulse shaper, threshold detector, pulse stretcher

One-shot : symbols

Nonretriggerable $t_w \simeq 30ns \cdot 0.7(2k\Omega) C_{EXT} \cdot 0.7 R_{EXT} C_{EXT}$



Retriggerable $t_w \simeq 45ns \cdot 0.32RC\left(1+\frac{0.7}{R}\right)$ where $R = 10k$

Astable Multivibrator